IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001]   This application is a divisional of application Serial No. 10/207,526, filed July 29, 2002, pending, which is related to U.S. Patent Application Serial No. 08/946,027 now U.S. Patent No. 6,190,972, issued February 20, 2001 and co-pending U.S. Patent Application Serial No. 09/651,858 now U.S. Patent No. 6,829,737, issued December 7, 2004.

Please amend paragraph number **[0003]** as follows:

[0003]   Semiconductor IC devices are manufactured on wafers or other bulk substrates of semiconductor material. Conventionally, many devices are manufactured on a single wafer and individual devices or groups of devices are singulated from the wafer and packaged. The IC devices are tested at various points during the manufacturing process, *i.e.*, with electrical probes while they are still on the wafer and then after packaging. The terms "IC", "IC," "device" and "IC device" are used interchangeably herein.

Please amend paragraph number **[0033]** as follows:

[0033]   Wafer level burn-in testing according to the present invention may begin with detecting the number of failures at time stamp t_0, prior to the first quarter of burn-in stressing. Detecting the number of failures at time stamp t_0 may be performed using BIST circuitry. The number of failures detected on the IC die and the time stamp may be recorded or stored in nonvolatile elements, such as antifuse registers, on the IC die itself. Then, the first quarter of burn-in stressing may be performed. At the end of the first quarter, t_1, the number of failures on the IC die is again detected (using BIST, for example) and stored in nonvolatile elements along with the time stamp, t_1. This procedure may be repeated for all four quarters of the wafer level burn-in testing, at which point the nonvolatile elements on each IC die contain wafer level burn-in burn-in testing data that may be used to generate burn-in reliability curves (bathtub curves). The nonvolatile elements may be fuses, antifuses or any other suitable nonvolatile storage elements.

Please amend paragraph number **[0034]** as follows:

[0034] FIG. 4 illustrates a bank 400 of nonvolatile registers suitable for use as the nonvolatile elements as described above. As shown in FIG. 4, the bank 400 may include five ~~8-bit~~ 8-bit registers, one for each time stamp, t_0-t_4. Each 8-bit register may include one bit for a time stamp and seven bits for storing the number of failures detected at the associated time stamp. The time stamp bit may be used, for example, by a state machine or incremental pointer that increments a pointer to the registers during the cycles of the burn-in testing so that the appropriate information is stored. The number of bits per register is not critical to the invention, as more or fewer bits may be used depending on the size of the memory array being tested or the quality of the manufacturing process. Generally, there may be $m + 1$ registers, each having n bits, where m and n are positive integers and m represents the number of cycles of burn-in testing. The physical arrangement of the bank 400 of nonvolatile registers and methods for storing information in and retrieving information from nonvolatile registers are within the knowledge of one of ordinary skill in the art and, thus, will not be further elaborated herein.

Please amend paragraph number **[0046]** as follows:

[0046] Wafer level burn-in circuitry 650 may also include address compression circuitry 606 which may be coupled to the memory array 612 and the BISS and BIST circuitry ~~14~~ ~~for~~ 614 for compressing cells of a memory array into redundancy space. Repairable failures can have variations in bit counts. Most memory IC dice are not prime (free from defects). Compression in redundancy space may occur for either column-repair space or row-repair space. For example, a 4Mb SRAM may be compressed into 1024 row-elements or 144 x 4 ~~column-elements.~~ column-elements. The size of the redundancy space (within the memory array) and the choice of column-repair space or row-repair space is usually based on various design, architectural, yield and real estate (die size) tradeoffs, all of which are within the knowledge of one of ordinary skill in the art and, thus, will not be further elaborated upon herein.

Please amend paragraph number **[0049]** as follows:

[0049]   Wafer level burn-in circuitry 650 of the present invention may be used in any higher order digital logic device or IC which may be suitable for wafer level burn-in to generate burn-in reliability curves. Memory device 600 may be, for example and not by way of limitation, a dynamic random access memory (DRAM), double data rate synchronous DRAM (DDR SDRAM), RAMBUS® DRAM (RDRAM®), extended data-out DRAM (EDO DRAM), fast-page-mode DRAM (FPM DRAM), static random access memory (SRAM), SyncBurst™ SRAM, Zero Bus Turnaround™ SRAM (ZBT™ SRAM), Quad Data Rate™ SRAM (QDR™ SRAM), double data rate synchronous SRAM (DDR SRAM) and nonvolatile electrically ~~block-erasable~~ block-erasable programmable read only memory (Flash).

Please amend paragraph number **[0051]** as follows:

[0051]   FIG. 8 is a block diagram of a system 800 for performing wafer level burn-in in accordance with the present invention. System 800 may include a high current VCC/VSS power supply 802 configured for providing power, VCC, and ground, VSS, to a wafer 804 during wafer level burn-in through a sacrificial metal layer on the wafer 804. System 800 may further include a high current power supply CMN 806 suitable for programming nonvolatile elements. High current power supply CMN 806 may also be used to provide a supervoltage that may be detected by supervoltage detection circuitry in each IC die. The supervoltage provides a logic signal to switch between a BISS mode and a BIST mode and for storing failures detected in nonvolatile elements (wafer level burn-in data) in accordance with the present invention. Wafer level ~~burn-in~~ burn-in data may be stored in nonvolatile elements (not shown) in each IC die (also not shown) on the wafer 804. Wafer 804 may be bulk semiconductor substrate 700 as described above with regard to FIG. 7. System 800 may further include a wafer probe tester 808 for reading the wafer level burn-in data to generate at least one wafer level burn-in reliability curve in accordance with the present invention. Wafer probe tester 808 may be used to effect repairs in each of the IC dice on the wafer 804 by programming in redundant elements.